J Electroceram (2009) 23:206–208
DOI 10.1007/s10832-007-9389-7

Dependence of hole mobility on channel surface of ultrathin-body silicon-on-insulator pMOSFETs

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Received: 11 June 2007 / Accepted: 4 December 2007 / Published online: 3 January 2008
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Abstract We investigated the characteristics of ultrathin-body (UTB) silicon-on-insulator (SOI) p-type metal–oxide–semiconductor field-effect transistors pMOSFETs with channel thickness less than 10 nm regime. At the same time, the dependence of electrical characteristics on the silicon surface orientations with (100) or (110) were also investigated. As a result, it is found that the electrical characteristics of (100)-surface UTB-SOI pMOSFETs were superior to those of (110)-surface. Moreover, the SOI thickness from 3 to 5 nm, the increase of effective hole mobility at the effective field of 0.3 MV/cm was observed for both (100) and (110) surfaces. The mobility enhancement ratio of (110) surface was larger than that of (100) surface.

Keywords Ultrathin-body · SOI · Hole mobility enhancement · Subband modulation

1 Introduction

Under sub-100 nm regime, conventional device has been confronted with several physical and essential limitations. As a result, a new device engineering to overcome these limits is strongly required. Ultrathin-body silicon-on-insulator metal–oxide–semiconductor field-effect transistor (UTB-SOI MOSFET) is considered as one of the most promising structure due to the short channel effects immunity. It has been reported theoretically and experimentally that electrons mobility was enhanced on (100) UTB-SOI nMOSFETs with channel thickness between 3 and 5 nm [1, 2]. The electron mobility enhancement was attributed to subband modulation in conduction band and reduction of inter-valley scattering [3, 4]. Several works has been reported on (110) channel pMOSFETs because the hole mobility in (110) channel surface is the highest [5, 6]. However, the mobility behavior of channel thickness under 10 nm UTB-SOI pMOSFETs has not yet been clarified.

In this paper, we investigated the hole mobility enhancement of UTB-SOI MOSFETs with channel thickness under 10 nm. At the same time, the dependence of electrical characteristics on the silicon surface orientation, such as (100) and (110), were also investigated.

2 Experimental

The fabrication procedure of the UTB-SOI pMOSFETs is summarized in Fig. 1. The UTB-SOI pMOSFETs with 2- to 20-μm channel-length were fabricated on p-type (100) and (110) unibond SOI wafers with a 100-nm top silicon layer. After initial RCA cleaning, the channel region was locally thinned by using the wet etching process to fabricate ultrathin channel region with the channel thickness (T_{SOI}) ranging from 10 to 1 nm. Each MOSFET devices on SOI wafer were isolated by mesa isolation structure. The gate oxide of 4-nm thickness was grown by thermal oxidation at 880°C in O_2 ambient. Sequentially, a 150-nm thickness in-situ phosphorus doped poly-Si film was deposited by low-pressure chemical vapor deposition at 650°C. Gate region was patterned by photolithography and reactive ion etching processes. Finally, the source and drain regions was doped by plasma doping of phosphorus at 450°C with an acceleration voltage of 3 keV [7].

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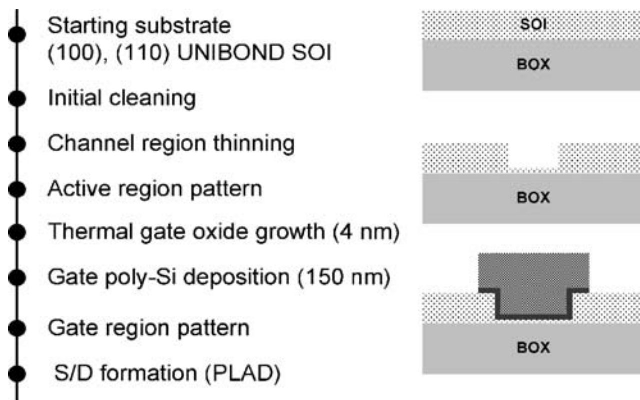

Fig. 1 Fabrication procedure of a UTB-SOI pMOSFETs device

3 Results and discussion

Figure 2 shows the top-Si thickness of SOI and root mean square (rms) roughness of Si surface after chemically etching of Si. The chemical etching of top-Si of SOI was carried out in 2.38% Tetramethy Ammonium Hydroxide (TMAH) solution. The thickness of Si channel was precisely controlled under 10 nm region using the (100) and (110)-orientation etching rate at room temperature of 2.44 and 1.67 nm/min, respectively. The rms roughness of surface was analyzed by atomic force microscope. The surface roughness of 4- and 8-nm thickness top-Si channel was 0.171 and 0.175 nm, respectively. Therefore, we confirmed that the surface roughness was almost unchanged by the chemical etching of silicon.

Figure 3 shows the cross sectional transmission electron microscope (TEM) images of fabricated UTB-SOI pMOS FET with a Si channel thickness of 6 nm. Thermal oxidation is frequently used in thinning process of SOI channel to obtain a high quality silicon surface. On the contrary, an

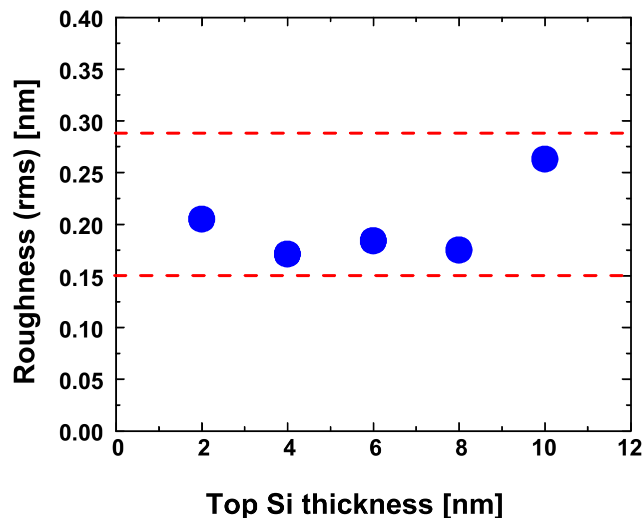

Fig. 2 Top-Si thickness of SOI and rms roughness of Si surface after chemical etching by TMAH solution

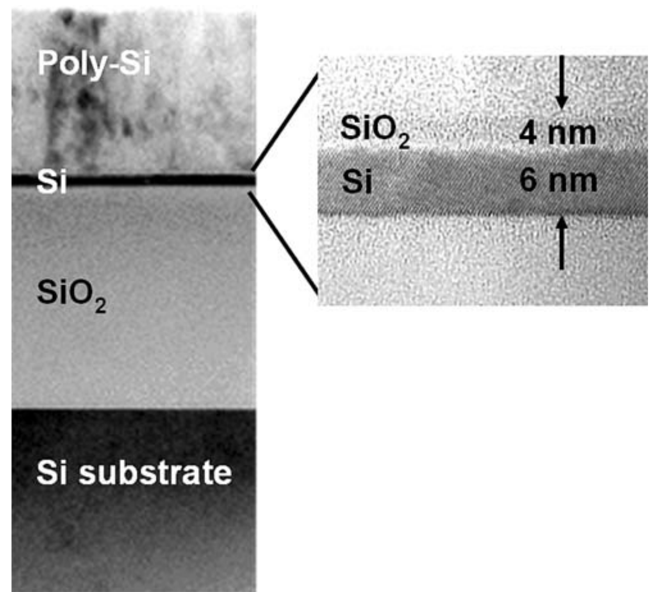

Fig. 3 Cross-sectional TEM images of UTB-SOI MOSFET

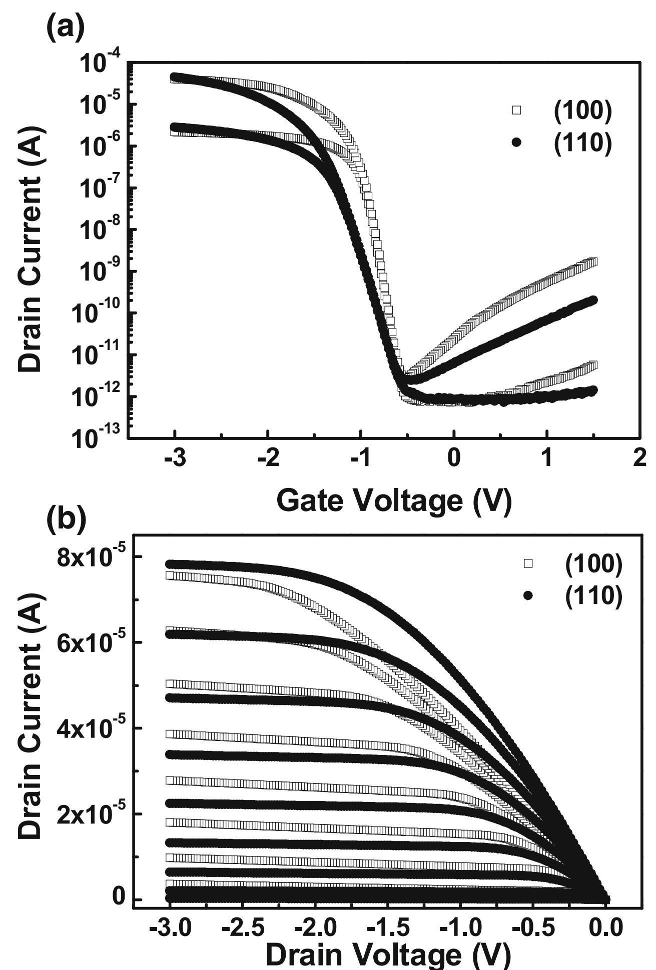

Fig. 4 I-V characteristics of UTB-SOI pMOSFETs; (**a**) subthreshold characteristics, (**b**) output current

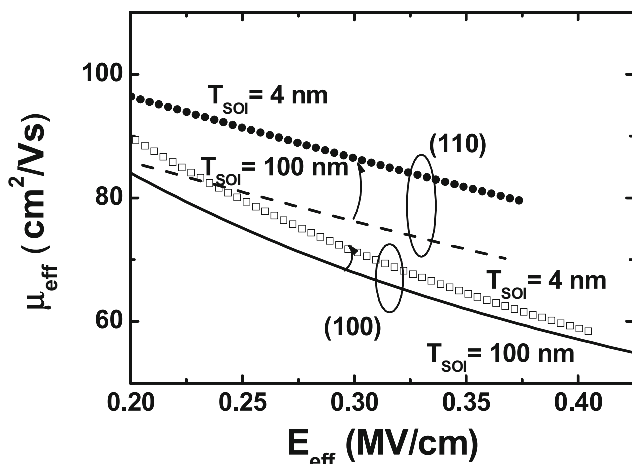

Fig. 5 Hole mobility characteristics of (100) and (110) surface UTB-SOI pMOSFETs

ultrathin Si channel with uniform thickness was able to obtain by simple wet etching process in this work.

The electrical measurements of the fabricated devices were performed by using the semiconductor parameter analyzer (HP 4156B). Figure 4 shows the electrical characteristics of UTB-SOI pMOSFETs. The subthreshold swing of (100) and (110) with 100 nm channel thickness were 75 and 130 mV/dec, respectively. The degradation of subthreshold swing for the (110) surface is associated with the high interface trap density between silicon channel and gate oxide. However, higher drive current in (110) channel was obtained due to higher hole mobility in (110) channel.

Figure 5 shows the hole mobility obtained from the (100) and (110) orientation channels. It is found that the hole mobility of 100 nm thinness (110) SOI pMOSFET is higher than that of the (100) surface at 0.3 MV/cm [8]. Especially, the mobility enhancement of hole was observed at 4 nm channel thickness. The mobility enhancement ratios of (100) and (110) channels are 1.73% and 13.68%, respectively. These mobility enhancements due to the band splitting in valance band are attributable to the reduction in averaged conductivity mass of hole as well as the suppression of inter-valley scattering between heavily hole band and lightly hole band.

Figure 6 shows the dependence of hole mobility enhancement ratio on the SOI channel thickness. It is found that the mobility decreased between 6 and 10 nm range due to the inter-valley and the intra-valley scattering. At 4 nm of channel thickness, however, the hole mobility of UTB-SOI pMOSFET increased. Moreover, mobility enhancement ratio of (110) surface was larger than that of (100) surface. Under 4 nm channel thickness, the hole mobility decreased both (100) and (110) surface due to the increasing inter-valley and intra-valley scatterings. Additionally, when the thickness of SOI is thinner than that of inversion layer, the hole mobility would be extremely degraded due to the increased surface roughness scattering.

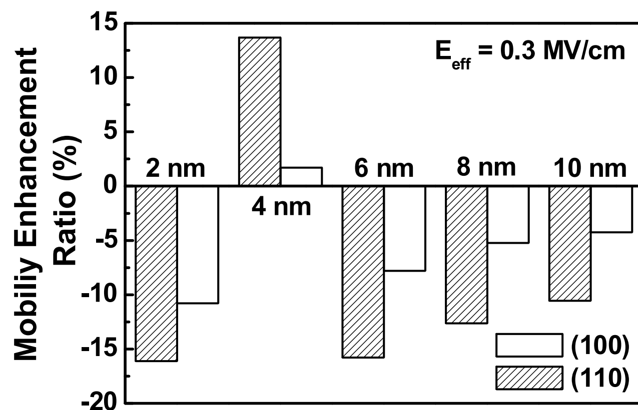

Fig. 6 Channel thickness dependency of mobility enhancement ratio on (100)- or (110)-surface channel UTB-SOI pMOSFETs

4 Conclusion

The UTB-SOI pMOSFETs with a channel thickness less than 10 nm were successfully fabricated by using simple and selective wet etching process. The subthreshold swing of (100) surface device was superior to that of (110) surface device due to lower interface trap density between channel and gate oxide. However, the hole mobility of (110) channel was larger than (100) channel SOI MOSFET with 100 nm channel thickness. When channel thickness is 4 nm, the hole mobility was enhanced both (100) and (110) surface UTB-SOI MOSFETs. Especially, (110) surface has large enhancement ratio than (100) surface. It is considered that such mobility enhancement can be attributed to the subband modulation by carrier confinement effects and the reduction of inter-valley scattering. Therefore, the UTB-SOI MOSFET less than 10 nm SOI channel thickness will provide a key solution for the sub-100 nm CMOS technology node.

Acknowledgements The present research has been conducted by the Research Grant of Kwangwoon University in 2007.

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